Abstracts

Load-Line Analysis in the Frequency Domain with Distributed Amplifier Design Examples

Time-Domain analysis of a multi-FET circuit over a wide frequency range and for several power levels using SPICE is not practical because of excessive computer time causing high cost and slow feedback to the designer. The load-line analysis to be described is a linear technique in the frequency domain and is therefore fast. A load-line ellipse is generated at each node of interest and graphically displayed and superimposed on the I-V curves of the device at that node. The driving signal to the amplifier and the amplifier matching networks are adjusted so that the load-line ellipse just fills the linear region of the FET I-V characteristics. Amplifier designs based on this approach agree with measured results within 0.5 dB at frequencies up to 18 GHz. What allows this technique to give accurate results is the sampling of the branch current "inside" the FET model while the FET parasitic are absorbed into the rest of the amplifier circuit.

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